Amendments to the Claims

Please amend Claims 1, 7, 12, 14 and 16. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

What we claim is:

1.   (Currently amended) A packet buffer random access memory (PBRAM) device, comprising:

        (a)   a memory array;

        (b)   a plurality of input ~~and output~~ ports to be coupled to a network controller device, the memory array for storing packet data received by the plurality of input ports being shared by the plurality of input ~~and output~~ ports; and

        (c)   a plurality of serial registers associated with the input ~~and output~~ ports, the serial registers simultaneously receiving packet data from the input ports and writing packet data to the memory array, the serial registers further being segmented into a plurality of segments, segments of respective serial registers being associated with corresponding portions of the memory array, segments of different serial registers simultaneously transferring packet data to different portions of the memory array.

2.   (Original) The PBRAM device of claim 1 wherein packet data is transferred into one segment of a serial register as data is simultaneously transferred out of another segment of the serial register.

3.   (Original) The PBRAM device of claim 1 wherein a portion of the memory array is a queue.

4.   (Original) The PRAM device of claim 3 wherein the queue includes a plurality of sub-queues, each sub-queue assigned a priority level.

5.   (Original) The PBRAM device of claim 4 wherein packet data is read from the sub-queue with the highest priority level that stores data.

6.   (Original) The PBRAM device of claim 1 wherein the memory array is a single global memory.

7.   (Currently amended) A method for storing data packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, the method comprising the steps of:

receiving a plurality of data packets from controllers coupled to said computer network at a plurality of input ports of the PBRAM device;

serially transferring portions of the data packets to different segments of serial registers that are connected between the input ports and a memory array, the memory array for storing packet data received by the input ports being shared by the plurality of input ports; and

conveying the portions of the data packets to different portions of the memory array in parallel, while concurrently transferring other portions of the packets to other segments of the serial registers.

8.   (Original) The method of claim 7 wherein a portion of the memory array is a queue.

9.   (Original) The method of claim 8 wherein the queue includes a plurality of sub-queues, each sub-queue assigned a priority level.

10.   (Original) The method of claim 9 wherein packet data is read from the sub-queue with the highest priority level that stores data.

11.   (Original) The PBRAM device of claim 7 wherein the memory array is a single global memory.

12.   (Currently amended) A packet buffer random access memory (PBRAM) device comprising:

a memory array;

a plurality of input ~~and output~~ ports coupled to the memory array by serial registers for conveying data to ~~and from~~ the memory array, the memory array for storing packet data received by the plurality of ports being shared by the plurality of input ~~and output~~ ports;

a plurality of command ports for receiving commands that indicate desired operations to be performed in relation to the data conveyed on the input ~~and output~~ ports; and

a memory management unit coupled between the ~~control~~ <u>command</u> ports and the memory array, said memory management unit establishing input queue structures within the memory array responsive to write commands issued on the command ports, the input queue structures for receiving pointers to locations in a packet table that point to the data that is conveyed from the input ports.

13.   (Original) The PBRAM device of claim 12 wherein the memory array is a single global memory.

14.   (Currently amended) A method for storing packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, <u>the method</u> comprising ~~the steps of~~:

receiving a packet from a controller coupled to said computer network by one of a plurality of input ports of said PBRAM device;

storing the packet in a physical location of a memory array of the PBRAM device, the memory array being shared by the plurality of input ports;

storing a pointer to the physical location in an entry of a packet table in the memory array;

storing a pointer to the entry in the packet table in an input queue structure, contained in the memory array of said PBRAM device; and

said input queue structure being further accessible by a plurality of output ports of said PBRAM device such that said pointer in the input queue structure is transferred to an associated output queue structure.

15.   (Original) The method of claim 14 wherein the output queue structure includes a plurality of sub-queue structures, each sub-queue structure assigned a priority level.

16.   (Currently amended) The method of claim 14 wherein packet data is read from [[the]] a sub-queue structure with [[the]] highest priority level that stores data.

17.   (Original) The PBRAM device of claim 14 wherein the memory array is a single global memory.

18.   (Original) An apparatus for storing packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, comprising:

means for receiving a plurality of packets from controllers coupled to said computer network by a plurality of input ports of the PBRAM device;

means for assigning input queue structures, contained in a memory array portion of the PBRAM device, to store packets, the memory array being shared by the plurality of input ports;

means for serially transferring portions of the packets to different segments of serial registers that are connected to the input ports and to the memory array;

means for conveying the portions of the packets to the memory array portion in parallel; and

means for storing said packets in said queue structures, said queue structures being further accessible by a plurality of output ports of said PBRAM device such that said input queue structures become output queue structures that deliver the packets to associated output ports.

19.   (Original) The apparatus of claim 18 wherein an output queue structure includes a plurality of sub-queues, each sub-queue assigned a priority level.

20.   (Original) The apparatus of claim 19 wherein packet data is read from the sub-queue with the highest priority level that stores data.

21.   (Original) The PBRAM device of claim 18 wherein the means for storing is a single global memory.

22.   (Original) An apparatus for storing packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, comprising:

      means for receiving a packet from a controller coupled to said computer network by one of a plurality of input ports of said PBRAM device;

      means for assigning an input queue structure, contained in a memory array portion of said PBRAM device, to store said packet, the memory array being shared by the plurality of input ports; and

      means for storing said packet in said queue structure, said queue structure being further accessible by a plurality of output ports of said PBRAM device such that said input queue structure becomes an output queue structure that delivers the packet to an associated output port.

23.   (Original) The apparatus of claim 22 wherein the output queue structure includes a plurality of sub-queue structures, each sub-queue assigned a priority level.

24.   (Original) The apparatus of claim 23 wherein packet data is read from the sub-queue structure with the highest priority level that stores data.

25.   (Original) The PBRAM device of claim 22 wherein the means for storing is a single global memory.